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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. FR999060

In Re Application Of: **Bonneau et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/745,988	12/21/2000	Moise, E.	23405	2136	1393

Invention: **BUILT-IN SELF TEST SYSTEM AND METHOD FOR HIGH-SPEED CLOCK AND DATA RECOVERY CIRCUIT**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Signature

Dated: **June 4, 2004**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Bonneau et al.	Confirmation No.:	1393
Serial No.:	09/745,988	Group Art Unit:	2136
Filed:	12/21/2000	Examiner:	Emmanuel Lionel Moise

Title: BUILT-IN SELF TEST SYSTEM AND METHOD FOR HIGH-SPEED CLOCK AND DATA RECOVERY CIRCUIT

CERTIFICATE OF MAILING

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To: Mail Stop Appeal Briefs – Patents
Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Dear Sir:

APPELLANTS' APPEAL BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

This is an appeal under 37 C.F.R. §1.191 and §1.192 from a Final Rejection, mailed on December 9, 2003, of claims 1-36, comprising all the claims finally rejected. A Notice of Appeal with a Request for One-Month Extension of Time was timely filed on April 5, 2004, and received in the U.S. Patent and Trademark Office on April 7, 2004, with an Appeal Brief due June 7, 2004. Therefore, this Brief is being timely filed. A Transmittal of Appeal Brief is

included herewith authorizing the Commissioner to charge the fee for filing this Appeal Brief in the amount of $330 as set forth in 37 C.F.R. §1.17(f).

REAL PARTY IN INTEREST

International Business Machines Corporation, the sole assignee of the inventors' rights in this patent application, is the real party in interest.

RELATED APPEALS AND INTERFERENCES

To the knowledge of Appellants, Appellants' undersigned legal representative, or the assignee, there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-23 were originally presented in the subject application. Claims 24-36 were added during prosecution. Claims 1-36 were finally rejected in a final Office Action with a mailing date of December 9, 2003, which was maintained in an Advisory Action with a mailing date of March 8, 2004. Therefore, claims 1-36 remain rejected and are the subject of this appeal.

STATUS OF AMENDMENTS

A Response to Final Office Action dated February 9, 2004 was filed. However, that Response contained only remarks with no amendments. All amendments made during prosecution have been entered and are reflected in the attached Appendix.

SUMMARY OF INVENTION

The present invention comprises a method and built-in system for testing a clock and data recovery circuit. Clock and data recovery circuits derive a clock signal from incoming digital data, so that the clock signal need not be sent with the data. In communications links, serializers on the transmitting end are used to serialize parallel data in a bit stream, while deserializers are used on the receiving end to parallelize the serial data stream. Test patterns can be used to test digital components. However, analog components are more problematic, and the present invention uses a built-in self-test approach.

The present invention is described with reference to FIGs. 2 and 3, and the descriptions thereof, at pages 9-12 of the specification. In the present invention, initial test data, comprising a frame header, is generated (204, 206; FIG. 2). The initial test data is input to a serializer (202; FIG. 2) for conversion into serial test data, which is sent to a clock and data recovery circuit (212; FIG. 2) for recovering the clock and test data from the serial test data. The recovered serial test data is input to a deserializer (214; FIG. 2) for conversion into recovered test data. The beginning portion of the recovered test data is compared to the frame header of the initial test data (216; FIG. 2). A match between the beginning portion of the recovered test data and the frame header indicates a positive outcome of the testing.

ISSUES

1. Whether the final Office Action improperly objected to the specification under 37 C.F.R. §1.75(d)(1) and MPEP §608.01(o) for allegedly filing to provide support for "beginning portion of the recovered test data."

2. Whether the final Office Action improperly rejected claims 24-28, 32, 33 and 35 under 35 U.S.C. §102(e) as allegedly anticipated by Schneider (U.S. Patent No. 6,201,829).

3. Whether the final Office Action improperly rejected claims 1-23, 29-31, 34 and 36 under 35 U.S.C. §103(a) as allegedly obvious over Schneider.

GROUPING OF CLAIMS

With respect to Issue No. 2 on appeal recited above, Appellants believe each of the following claim sets to be separately patentable over the prior art cited in the §102(e) rejection thereof:

claim 24 (claims 25-28, 32, 33 and 35 stand or fall with claim 24).

With respect to Issue No. 3 on appeal recited above, Appellants believe each of the following claim sets to be separately patentable over the prior art cited in the §103 rejection thereof:

claim 1 (claims 2-7, 9-12, 14, 15, 17, 19, 22, 23, 29, 30 and 34 stand or fall with claim 1);

claim 8 (claims 13, 31 and 36 stand or fall with claim 8);

claim 16 (claim 21 stands or falls with claim 16); and

claim 18 (claim 20 stands or falls with claim 18).

ARGUMENT

Issue No. 1

The Examiner objected to the specification as allegedly failing to provide proper antecedent basis for claim language that includes "beginning portion of the recovered test data" (e.g., claim 1). It is well settled that support for a claim limitation need not be express, but may be implied from the specification, drawings and even the claims as filed.

Appellants respectfully submit that adequate support for this language is provided at, for example, p. 9, lines 6-24 and p. 11, lines 2-5 of Appellants' specification. Initially, Appellants note that these sections describe both the initial test data and the recovered test data as being "patterns." For instance, p. 9, lines 12-15 refer to "the initial test data generated by the pattern generator" and a comparison of that initial test data to "recovered data" rebuilt by a deserializer. This comparison is also described at p. 11, lines 2-5, which clarifies that the recovered data is also a pattern: "A second counter allows during a predefined period of time that numerous test patterns be repetitively generated as long as the recovered test patterns do not match the expected ones" (emphasis added). Further, these patterns are defined at p. 9, lines 16-18:

> The patterns are predefined to be made of a frame header signature followed by sequence of bits containing a maximum number of transitions such as '01010101...'.

Since a pattern in this context is composed of a frame header signature followed by a sequence of bits with maximum transitions, the frame header signature is clearly the beginning portion of the pattern. It then follows that the particular types of patterns, such as the recovered test data, also include a beginning portion, which is the frame header signature.

To summarize the logical steps:

- "recovered test data" described as "pattern"
- pattern = frame header signature followed by sequence of bits
- frame header signature is the beginning portion of the pattern
- thus, "recovered test data" includes a frame header signature

Therefore, appellants submit that the specification provides adequate support for the phrase "beginning portion of the recovered test data."

Issue No. 2

The final Office Action rejected claims 24-28, 32-33 & 35 under 35 U.S.C. §102(e), as allegedly anticipated by Schneider (U.S. Patent No. 6,201,829).

Claim 24 recites a built-in self test circuit for testing a clock and data recovery circuit. The circuit includes: (1) data generating means for generating a test data byte; (2) serializing means coupled to the data generating means for converting the test data byte into serial test data; (3) clock and data recovery means (hereinafter, "CDR") coupled to the output of the serializing means for recovering the clock and test data from the serial test data; (4) deserializing means coupled to the output of the clock and data recovery means for converting the recovered serial test data into a recovered test data byte; and (5) analyzing means connected to the output of the deserializing means for comparing the recovered test data byte to the test data byte, wherein an

outcome of the testing comprises indicating improper operation of the clock and data recovery means.

The final Office Action alleges at page 3 that Appellants' claimed element of "wherein an outcome of the testing comprises indicating improper operation of the clock and data recovery means" is inherent in Schneider.

The doctrine of inherency is well-settled in patent law, and is best described in an excerpt from *Hansgirg v. Kemmer*, 26 C.C.P.A. 937, 102 F.2d 212, 40 U.S.P.Q. 665 (1939):

> Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. [citations omitted.] If, however, the disclosure [of the cited reference] is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient [to anticipate the claimed invention].

Id. at 940, 102 F.2d at 214, 40 U.S.P.Q. at 667; *Stoller v. Ford Motor Co.*, 18 U.S.P.Q.2d 1545, 1547 (Fed. Cir. 1991); *Tyler Refrigeration v. Kysor Industrial Corporation*, 227 U.S.P.Q. 845, 847 (Fed. Cir. 1985); *Ex parte Levy,* 17 U.S.P.Q.2d 1461, 1464 (B.P.A.I. 1990); *In re Oelrich and Divigard*, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981).

In *Ex parte Levy*, the court stated that "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." *Ex parte Levy*, 17 U.S.P.Q.2d at 1464 (lengthy citation omitted) (underlining added).

The final Office Action cites col. 9, lines 8-9 and col. 9, line 35 as supporting the alleged inherency. The first cited section states that the functionality of the transceiver is tested with regard to operation and speed. Appellants respectfully submit that the phrase "with regard to operation and speed" refers to testing done while the transceiver circuit is in operation and is operating at speed. This is more clearly asserted at col. 5, lines 63-67 of Schneider, which states that the signature analyzer returning a match signal indicates "that the transceiver circuit is able to serialize and deserialize 10-bit wide transmission character information at its nominal 1.06 GHz operational frequency" (see also col. 5, lines 15-18; col. 8, lines 64-67; col. 9, lines 12-16; col. 10, lines 57-60; and col. 11, lines 3-6). Thus, the signature analyzer's comparison does not describe or even suggest an improper operation of the CDR in particular. Instead, the analyzer in Schneider indicates the ability of the transceiver circuit to serialize and deserialize. If this indication suggests the operability of any particular components of the transceiver (and Appellants are not at all convinced that it does), Appellants submit that those components would be the serializer and/or deserializer, which are both different from the CDR (see FIG. 5 thereof, wherein serializer 52 and deserializer 58 are distinct from the phase lock loop 48).

Further, the second section cited in support of the alleged inherency merely states that all the clock inputs are tied to REFCLK (col. 9, line 35). REFCLK is a 106.25 MHz clock signal, which is a frequency equal to the operational speed of the input latch of the transceiver chip (col. 9, lines 35-38). This clock signal allows the linear feedback shift register (LFSR) to generate 10-bit test patterns that may be processed as though they were conventional transmission characters (col. 10, lines 11-13 & 34-46). Appellants respectfully submit that this section of Schneider addresses a specific frequency of a clock input that is an assumed condition of the test process.

It does not teach or suggest that an outcome of testing comprises indicating improper operation of the CDR.

For the reasons stated above, Appellants respectfully submit that the Office Action does not provide a basis in fact and/or technical reasoning that reasonably supports a determination that the improper operation of the CDR necessarily flows from the teachings of Schneider. Thus, Appellants submit that that the rejection fails to present a proper case of inherency, and independent claim 24 cannot be anticipated by Schneider.

Issue No. 3

The Office Action rejected claims 1-23, 29-31, 34 & 36 under 35 U.S.C. §103(a), as allegedly obvious over Schneider. Appellants respectfully, but most strenuously, traverse this rejection.

Claim 1 recites a technique for testing a clock and data recovery (CDR) circuit, which includes, for example, generating test data that comprises a frame header; converting the test data into serial test data; recovering the clock and test data from the serial test data; converting the recovered serial test data into recovered test data; and comparing a beginning portion of the recovered test data to the frame header. A match between the beginning portion of the recovered test data and the frame header indicates a positive outcome of the testing of the CDR circuit.

While the final Office Action admits that Schneider "fails to explicitly disclose [indicating] a successful testing based on whether there is a match between the beginning portion of the recovered test data and the frame header[,]" it is alleged therein that it would be obvious to

do so in light of one skilled in the art knowing of the trade-off that exists in doing a "whole to whole comparison" and a comparison using only part of the data. Appellants submit that the allegation fails to present even a *prima facie* case, and that there must be some teaching, suggestion or incentive within the reference itself to make the leap alleged to be so obvious (see case law cited below).

Appellants submit the final Office Action lists in hindsight the modification utilizing a comparison with the beginning portion of the recovered test data. However, noticeably absent from the final Office Action is any express teaching, suggestion or incentive identified in the art itself for the proposed modification. It is well-settled that obviousness based on separate elements existing in multiple prior art references cannot be established absent some teaching or suggestion, in the prior art, to combine the elements. A similar rationale applies to establishing obviousness based on a single reference. For example, *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1316-17 (Fed. Cir. 2000) holds that:

> Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference.

The only justification given for the modification is the following language on page 5 of the final Office Action:

> However, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to implement the claimed invention because one of ordinary skill in the art know of the trade-off that exists in doing a "whole to whole comparison" and a comparison using just part of the data. One is more compact and leads sometimes to better results while the other is faster and may use less hardware.

This reasoning does not point to any particular discussion in Schneider and does not serve as the required showing of a suggestion or motivation to modify the teachings of Schneider as proposed by the final Office Action. Moreover, there is no support given for the allegation that one of ordinary skill in the art would know of the "trade-off." Appellants do not concede this point.

Even assuming, *arguendo*, that the final Office Action provided the requisite showing of a suggestion or motivation to modify Schneider, Appellants submit that the proposed modification is improper, since Schneider's test pattern generation in accordance with the standard Fibre Channel 8B/10B transmission protocol teaches away from the proposed comparison using only a beginning portion of recovered test data. As valid transmission characters in the 8B/10B encoding scheme, the predefined test patterns in Schneider are transmitted as 10-bit patterns (i.e., 10-bit "transmission characters"; see col. 4, line 61 – col. 5, line 2). Further, no fewer than 10 bits in each pattern are necessary to provide inversion at the first and sixth bits, and to generate at least 255 unique patterns conforming to the 8B/10B protocol (col. 5, lines 19-50). Since the comparison of patterns in Schneider depends on their 10-bit based uniqueness, Schneider teaches away from the proposed modification that would use fewer than 10 bits (i.e., a beginning portion of the recovered test data).

Therefore, Appellants submit that claim 1 cannot be rendered obvious over Schneider.

Claim 8 recites that the data generating means is a programmable data generator.

Against claim 8, the final Office Action admits at page 7 that "Schneider does not explicitly disclose that the data generating means is a programmable data generator."

Nonetheless, the final Office Action alleges that "it would have been obvious ... because doing so would have provided a more versatile generator." Appellants submit this again fails to present even a *prima facie* case for obviousness.

Even ignoring the lack of a *prima facie* case, however, Appellants submit there is no teaching or suggestion in Schneider of a programmable data generator. In fact, since Schneider only requires a set pattern for the test data, there is no need in Schneider for programmability, since the test pattern does not need to change from test to test.

Therefore, Appellants submit that claim 8 cannot be rendered obvious over Schneider.

Claim 16 recites an initial step of waiting for a predetermined period of time to allow the phase lock loop to lock to a predetermined frequency before beginning the generating (of test data).

Against claim 16, the final Office Action alleged at page six that "the phase lock loop in Schneider's circuit inherently waits for a predetermined period before being allowed to lock to a predetermined frequency."

Appellants submit there is no teaching or suggestion in Schneider of either PLL's (elements 40 and 48 in FIG. 5) waiting a predetermined period of time before locking. Appellants submit that while any PLL necessarily locks after a non-zero time (obviously PLL's cannot instantaneously lock), that time is not inherently a *predetermined* time. The two are really quite different things, which Appellants submit the final Office Action overlooks.

Therefore, Appellants submit that claim 16 cannot be rendered obvious over Schneider.

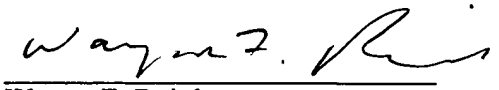
Claim 18 recites that the generating and repeating (of claim 17) are performed until a counter reaches a predetermined number of pulses.

The final Office Action admits on page seven that "Schneider does not explicitly disclose the use of a counter included within the state machine to count the number of pulses." Nonetheless, the final Office Action alleges that one skilled in the art would have implemented this aspect, "because the use of counter/s in state machines is well known in the art." While Appellants are not at all convinced that such is the case (no evidence was provided), the mere existence of counters does not itself teach or suggest the use of one to test until a predetermined number of pulses is reached.

Therefore, Appellants submit that claim 18 cannot be rendered obvious over Schneider.

CONCLUSION

In conclusion, Appellants submit that the specification provides adequate support for the claimed phrase "beginning portion of the recovered test data," that claim 24 is not anticipated by Schneider, and that none of claims 1, 8, 16 or 18 is obvious over Schneider. Therefore, Appellants submit that the final Office Action should be reversed in all respects.



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Dated: June 4, 2004.

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APPENDIX

1. A built-in self test circuit for testing a clock and data recovery circuit comprising:

data generating means for generating test data, wherein the test data comprises a frame header;

serializing means coupled to the data generating means for converting the test data into serial test data;

clock and data recovery means coupled to the output of the serializing means for recovering the clock and test data from the serial test data;

deserializing means coupled to the output of the clock and data recovery means for converting the recovered serial test data into recovered test data; and

analyzing means connected to the output of the deserializing means for comparing a beginning portion of the recovered test data to the frame header,

wherein a match between the beginning portion of the recovered test data and the frame header indicates a positive outcome of said testing.

2. The circuit of claim 1 wherein said clock and data recovery means comprises a phase lock loop.

3. The circuit of claim 2 further comprising a multiplexer coupled to the clock and data recovery means for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

4. The circuit of claim 2 further comprising a first multiplexer coupled to the serializing means for inputting operational parallel data or said test data upon setting of a data selection signal (B-ENB).

5. The circuit of claim 4 further comprising a second multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

6. The circuit of claim 5 wherein said test data is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

7. The circuit of claim 6 further comprising a state machine to control said generating means and said analyzing means.

8. The circuit of claim 7 wherein said data generating means is a programmable data generator.

9. The circuit of claim 1 further comprising a multiplexer coupled to the serializing means for inputting operational parallel data or said test data upon setting of a data selection signal (B-ENB).

10. The circuit of claim 1 further comprising a multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

11. The circuit of claim 1 wherein said test data is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

12. The circuit of claim 1 further comprising a state machine to control said generating means and said analyzing means.

13. The circuit of claim 1 wherein said data generating means is a programmable data generator.

14. A method for testing a clock and data recovery circuit comprising:

generating initial test data, wherein the initial test data comprises a frame header;

inputting the initial test data to a serializer for conversion into serial test data;

sending the serial test data to the clock and data recovery circuit for recovering the clock and test data from the serial test data;

inputting the recovered serial test data to a deserializer for conversion into recovered test data; and

comparing a beginning portion of the recovered test data to the frame header,

wherein a match between the beginning portion of the recovered test data and the frame header indicates a positive outcome of said testing.

15. The method of claim 14 wherein said clock and data recovery circuit comprises a phase lock loop.

16. The method of claim 15 further comprising an initial step of waiting for a predetermined period of time to allow said phase lock loop to lock to a predetermined frequency before beginning of said generating.

17. The method of claim 16 further comprising:

generating new test data; and

repeating said serializing, recovering, deserializing and comparing until the beginning portion of the recovered test data matches the frame header.

18. The method of claim 17 wherein said generating new test data and said repeating are performed until a counter reaches a predetermined number of pulses.

19. The method of claim 18 wherein said generating and said comparing are controlled by a state machine.

20. The method of claim 19 wherein said counter is included within said state machine.

21. The method of claim 14 further comprising an initial step of waiting for a predetermined period of time to allow said phase lock loop to lock to a predetermined frequency before beginning of said generating.

22. The method of claim 14 further comprising:

generating new test data; and

repeating said serializing, recovering, deserializing and comparing until the beginning portion of the recovered test data matches the frame header.

23. The method of claim 14 wherein said generating and said comparing are controlled by a state machine.

24. A built-in self test circuit for testing a clock and data recovery circuit comprising:

data generating means for generating a test data byte;

serializing means coupled to the data generating means for converting the test data byte into serial test data;

clock and data recovery means coupled to the output of the serializing means for recovering the clock and test data from the serial test data;

deserializing means coupled to the output of the clock and data recovery means for converting the recovered serial test data into a recovered test data byte; and

analyzing means connected to the output of the deserializing means for comparing the recovered test data byte to the test data byte,

wherein an outcome of said testing comprises indicating improper operation of the clock and data recovery means.

25. The circuit of claim 24 wherein said clock and data recovery means comprises a phase lock loop.

26. The circuit of claim 25 further comprising a multiplexer coupled to the clock and data recovery means for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

27. The circuit of claim 25 further comprising a first multiplexer coupled to the serializing means for inputting operational data byte or said test data byte upon setting of a data selection signal (B-ENB).

28. The circuit of claim 27 further comprising a second multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

29. The circuit of claim 28 wherein said test data byte is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

30. The circuit of claim 29 further comprising a state machine to control said generating means and said analyzing means.

31. The circuit of claim 30 wherein said data generating means is a programmable data generator.

32. The circuit of claim 24 further comprising a multiplexer coupled to the serializing means for inputting operational data byte or said test data byte upon setting of a data selection signal (B-ENB).

33. The circuit of claim 24 further comprising a multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

34. The circuit of claim 24 wherein said test data byte is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

35. The circuit of claim 24 further comprising a state machine to control said generating means and said analyzing means.

36. The circuit of claim 24 wherein said data generating means is a programmable data generator.